

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: T. HOTTA, et al

Serial No.: Not yet assigned

Filing Date: November 6, 2003

For: DATA PROCESSING SYSTEM GENERATING CLOCK SIGNAL FROM AN  
INPUT CLOCK PHASE LOCKED TO THE INPUT CLOCK AND USED FOR  
CLOCKING LOGIC DEVICES

**LETTER CLAIMING RIGHT OF PRIORITY**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

November 6, 2003

Sir:

Under the provisions of 35 USC 119 and 37 CFR 1.55, applicants hereby claim the right  
of priority based on:

**Japanese Application No. 62/101930**  
**Filed: April 27, 1987**

**Japanese Application No. 62/181060**  
**July 22, 1987**

Certified copies of said application documents were filed in parent application Serial No.  
07/184,782, filed April 22, 1988, now U.S. Patent No. 5,133,064, said certified documents filed  
in the United States Patent and Trademark Office on February 4, 1992. Acknowledgement  
thereof is respectfully requested.

Respectfully submitted,



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CIB/jdc  
Enclosures  
703/312-6600

日 本 国 特 許 庁

PATENT OFFICE  
JAPANESE GOVERNMENT

付の書類は下記の出願書類の謄本に相違ないことを証明する。  
to certify that the annexed is a true copy of the following application as filed  
Office.

年 月 日      1 9 8 7 年 4 月 2 7 日  
Application:

番 号      昭 和 6 2 年 特 許 願 第 1 0 1 9 3 0 号  
Application Number:

願 人      株 式 会 社 日 立 製 作 所  
Applicant(s):

1 9 8 8 年 5 月 2 7 日

特 許 庁 長 官  
Director-General,  
Patent Office

小 川 邦 夫



出 証 昭      6 3 - 2 6 0 5 7